

## UTKAL INSTITUTE OF ENGINEERING \& TECHNOLOGY

| DISCIPLINE: <br> ETC | DISCIPLINE: $3^{\text {rd }} \text { Sem }$ | NAME OF THE TEACHING FACULTY: Er.Jyoti Prakash Swain |  |  |
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| SUBJECT: <br> DIGITAL <br> ELECTRONICS | No of Days/Per week class allotted: 4 Class P/W(60) | Semester From Date:15/09/2022 <br> To Date:22/12/2022 <br> No. Of Weeks: 15 |  |  |
| WEEK | WEEK | WEEK | REMARKS |  |
| $1^{\text {st }}$ | $1^{\text {st }}$ | Number System-Binary, Octal, Decimal, Hexadecimal Conversion from one system to another number system. | Date | Dean/Principal |
|  | $2^{\text {nd }}$ | Number System-Binary, Octal, Decimal, Hexadecimal Conversion from one system to another number system. |  |  |
|  | $3^{\text {rd }}$ | Number System-Binary, Octal, Decimal, Hexadecimal Conversion from one system to another number system. |  |  |
|  | $4^{\text {th }}$ | Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1's \& 2's complement of Binary numbers\& Subtraction using complements method |  |  |
| $2^{\text {nd }}$ | $1^{\text {st }}$ | Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1's \& 2's complement of Binary numbers\& Subtraction using complements method |  |  |
|  | $2^{\text {nd }}$ | Doubt Clear Class |  |  |
|  | $3^{\text {rd }}$ | Doubt Clear Class |  |  |
|  | $4^{\text {th }}$ | Doubt Clear Class |  |  |


| $3^{\text {rd }}$ | $1^{\text {st }}$ | Digital Code \& its application \& distinguish between weighted \& non-weight Code, Binary codes, excess-3 and Gray codes. |  |
| :---: | :---: | :---: | :---: |
|  | $2^{\text {nd }}$ | Digital Code \& its application \& distinguish between weighted \& non-weight Code, Binary codes, excess-3 and Gray codes. |  |
|  | $3^{\text {rd }}$ | Digital Code \& its application \& distinguish between weighted \& non-weight Code, Binary codes, excess-3 and Gray codes. |  |
|  | $4^{\text {th }}$ | Logic gates: <br> AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR-Symbol, Function, expression, truth table \& timing diagram |  |
| $4^{\text {th }}$ | $1^{\text {st }}$ | Revision of last few class |  |
|  | $2^{\text {nd }}$ | Revision of last few class |  |
|  | $3{ }^{\text {rd }}$ |  |  |
|  | $4^{\text {th }}$ | Universal Gates\& its Realisation |  |
| $5^{\text {th }}$ | $1^{\text {st }}$ | Universal Gates\& its Realisation |  |
|  | $2^{\text {nd }}$ | Boolean algebra, Boolean expressions, Demorgan's Theorems. |  |
|  | $3^{\text {rd }}$ | Boolean algebra, Boolean expressions, Demorgan's Theorems. |  |
|  | $4^{\text {th }}$ | Boolean algebra, Boolean expressions, Demorgan's Theorems. |  |
| $6^{\text {th }}$ | $1^{\text {st }}$ | Revision of Last Class |  |
|  | $2^{\text {nd }}$ | Revision of Last Class |  |
|  | $3^{\text {rd }}$ | Represent Logic Expression: SOP \& POS forms |  |
|  | $4^{\text {th }}$ | Represent Logic Expression: SOP <br> \& POS forms |  |
|  | $1^{\text {st }}$ | Karnaugh map (3 \& 4 Variables)\&Minimization of logical expressions, don't care conditions |  |


| $7^{\text {th }}$ | $2^{\text {nd }}$ | Karnaugh map (3 \& 4 <br> Variables)\&Minimization of logical expressions ,don't care conditions |  |  |
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|  | $3^{\text {rd }}$ | Karnaugh map (3 \& 4 <br> Variables)\&Minimization of logical expressions , don't care conditions |  |  |
|  | $4^{\text {th }}$ | Assignment |  |  |
| $8^{\text {th }}$ | $1^{\text {st }}$ | Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder. |  |  |
|  | $2^{\text {nd }}$ | Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder. |  |  |
|  | $3^{\text {rd }}$ | Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit) |  |  |
|  | $4^{\text {th }}$ | Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit) |  |  |
| $9^{\text {th }}$ | $1^{\text {st }}$ | Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above) |  |  |
|  | $2^{\text {nd }}$ | Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above) |  |  |
|  | $3^{\text {rd }}$ | Revision Class |  |  |
|  | $4^{\text {th }}$ | Principle of flip-flops operation, its Types |  |  |
| $10^{\text {th }}$ | $1^{\text {st }}$ | Principle of flip-flops operation, its Types |  |  |
|  | $2^{\text {nd }}$ | Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications |  |  |
|  | $3^{\text {rd }}$ | C l o c k e d SR,D,JK,T,JK Master <br> Slave flip-flops-Symbol, logic <br> Circuit, truth table and applications |  |  |



| $14^{\text {th }}$ | $1^{\text {st }}$ | Characteristics of Digital ICsPropagation Delay, fan-out, fanin, Power Dissipation ,Noise Margin ,Power Supply requirement \&Speed with Reference to logic families |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $2^{\text {nd }}$ | Characteristics of Digital ICsPropagation Delay, fan-out, fanin, Power Dissipation ,Noise Margin ,Power Supply requirement \&Speed with Reference to logic families |  |  |
|  | $3^{\text {rd }}$ | Last class Discussion |  |  |
|  | $4^{\text {th }}$ | Last class Discussion |  |  |
| $15^{\text {th }}$ | $1^{\text {st }}$ | Last class Discussion |  |  |
|  | $2^{\text {nd }}$ | Discussion Sample paper question |  |  |
|  | $3^{\text {rd }}$ | Discussion Sample paper question |  |  |
|  | $4^{\text {th }}$ | Discussion Sample paper question |  |  |



HOD

Chittankian Parida
DEAN


PRINCIPAL

